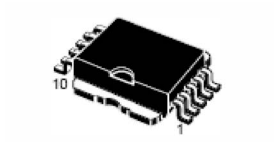
VN920SP-E

High-side driver

Features

Type	$R_{DS(on)}$	I_{OUT}	V_{CC}
VN920SP-E	15 mΩ	30 A	36 V

- ECOPACK®: lead free and RoHS compliant
- Automotive Grade: compliance with AEC guidelines
- Very low standby current
- CMOS compatible input
- Proportional load current sense
- Current sense disable
- Thermal shutdown protection and diagnosis
- Undervoltage shutdown
- Overvoltage clamp
- Load current limitation



Description

The VN920SP-E is a monolithic device designed in STMicroelectronics™ VIPower™ M0-3 technology. The VN920SP-E is intended for driving any type of load with one side connected to ground. The active V_{CC} pin voltage clamp protects the device against low energy spikes (see ISO7637 transient compatibility table). Active current limitation combined with thermal shutdown and automatic restart protects the device against overload.

The device integrates an analog current sense output which delivers a current proportional to the load current. The device automatically turns-off in the case where the ground pin becomes disconnected.

Table 1. Device summary

Package	Order codes	
	Tube	Tape and reel
PowerSO-10™	VN920SP-E	VN920SPTR-E

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1 Block diagram and pin description

Figure 1. Block diagram

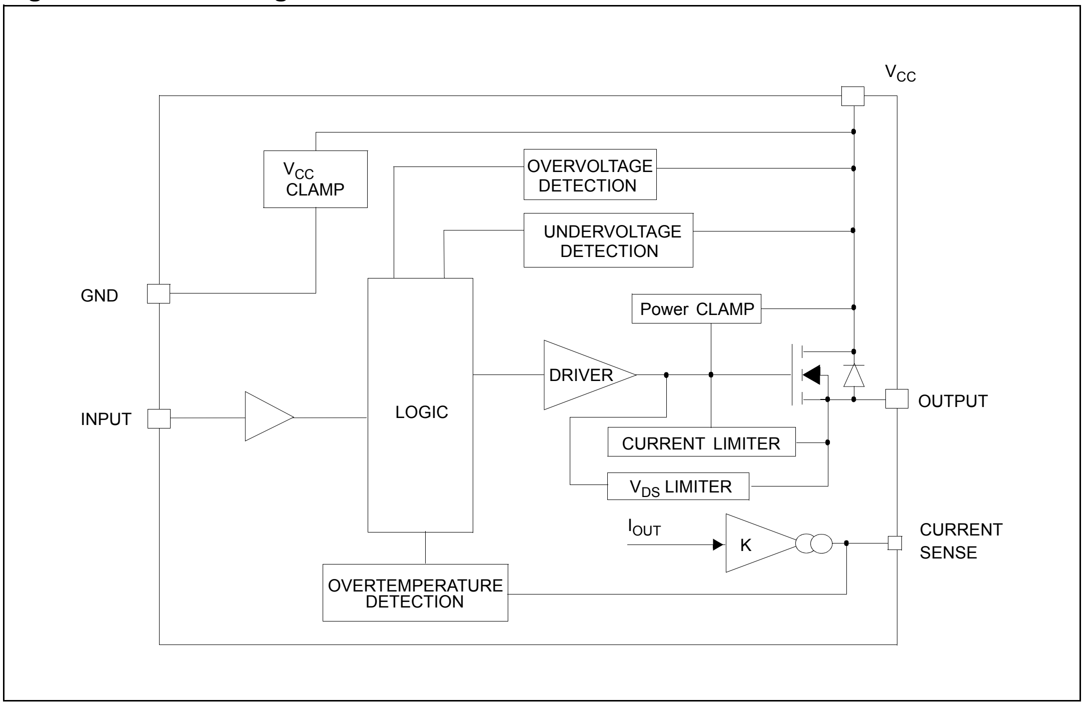


Figure 2. Configuration diagram (top view)

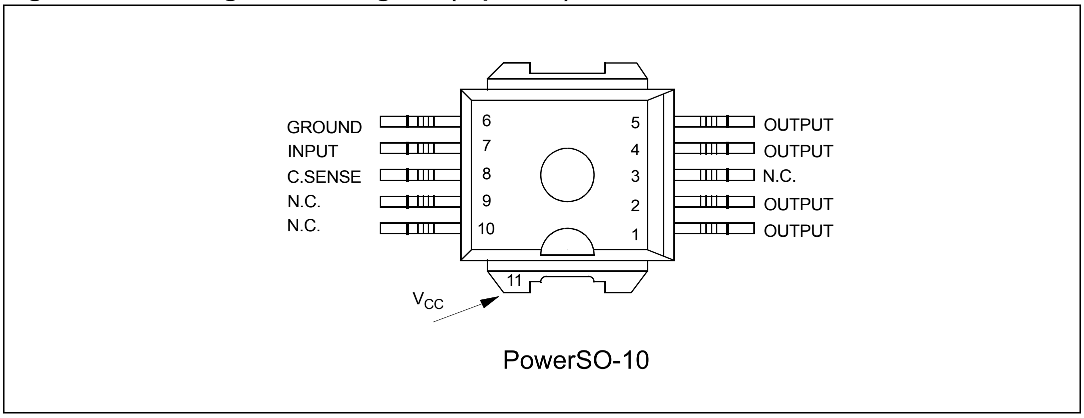
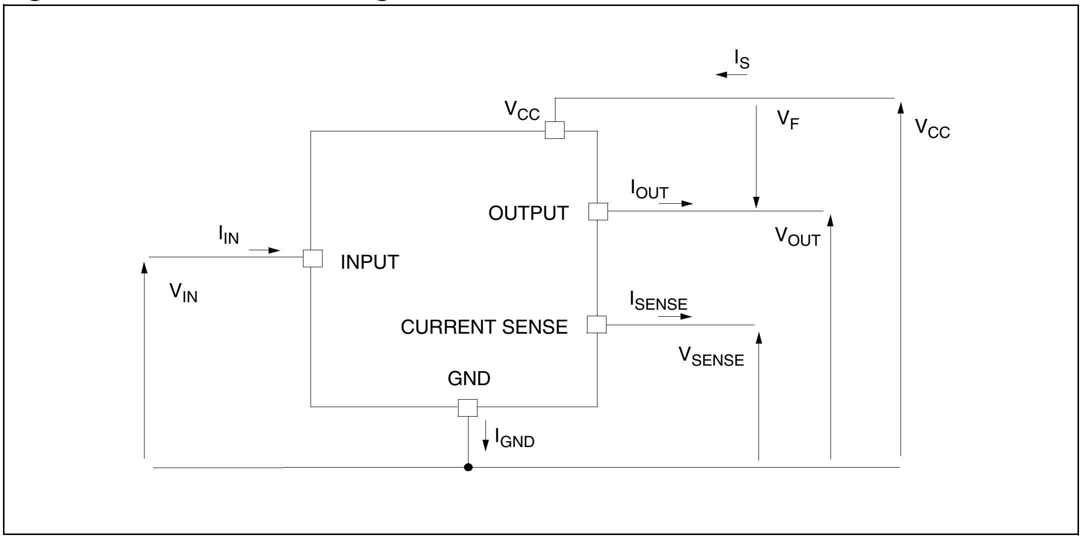


Table 2. Suggested connections for unused and not connected pins

Connection / pin	Current sense	N.C.	Output	Input
Floating		X	X	X
To ground	Through 1 KΩ resistor	X		Through 10KΩ resistor

2 Electrical specifications

Figure 3. Current and voltage conventions



2.1 Absolute maximum ratings

Stressing the device above the rating listed in *Table 3* may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics sure program and other relevant quality document.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	41	V
$-V_{CC}$	Reverse DC supply voltage	-0.3	V
$-I_{GND}$	DC reverse ground pin current	-200	mA
I_{OUT}	DC output current	Internally limited	A
$-I_{OUT}$	Reverse DC output current	-40	A
I_{IN}	DC input current	+/-10	mA
V_{CSENSE}	Current sense maximum voltage	-3 +15	V V
V_{ESD}	Electrostatic discharge (Human Body Model: R = 1.5 KΩ; C = 100 pF) – INPUT – CURRENT SENSE – OUTPUT – V_{CC}	 4000 2000 5000 5000	 V V V V

Table 3. Absolute maximum ratings (continued)

Symbol	Parameter	Value	Unit
E_{MAX}	Maximum switching energy (L = 0.25 mH; R_L= 0 Ω; V_{bat} = 13.5 V; T_{jstart} = 150 °C; I_L = 45 A)	362	mJ
P_{tot}	Power dissipation $T_C \leq$ 25 °C	96.1	W
T_j	Junction operating temperature	Internally limited	°C
T_c	Case operating temperature	-40 to 150	°C
T_{STG}	Storage temperature	-55 to 150	°C

2.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Max. value		Unit
$R_{thj-case}$	Thermal resistance junction-case (max)	1.3		°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient (max)	51.3(1)	37(2)	°C/W °C/W

1. When mounted on FR4 printed circuit board with 0.5 cm^2 of Cu (at least 35 µm thick).
2. When mounted on FR4 printed circuit board with 6 cm^2 of Cu (at least 35 µm thick).

2.3 Electrical characteristics

Values specified in this section are for 8 V < V_{CC} < 36 V; -40 °C < Tj < 150 °C, unless otherwise stated.

Table 5. Power

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating supply voltage		5.5	13	36	V
V_{USD}	Undervoltage shutdown		3	4	5.5	V
V_{OV}	Overvoltage shutdown		36			V
R_{ON}	On-state resistance	I_{OUT} = 10 A; T_j = 25 °C; I_{OUT} = 10 A; I_{OUT} = 3 A; V_{CC} = 6 V			15 30 50	mΩ mΩ mΩ
V_{CLAMP}	Clamp voltage	I_{CC} = 20 mA(1)	41	48	55	V
I_S	Supply current	Off-state; V_{CC} = 13 V; V_{IN} = V_{OUT} = 0 V Off-state; V_{CC} = 13 V; V_{IN} = V_{OUT} = 0 V; T_j = 25 °C On-state; V_{CC} = 13 V; V_{IN} = 5 V; I_{OUT} = 0 A; R_{SENSE} = 3.9 kΩ		10 10	25 20 5	µA µA mA
$I_{L(off1)}$	Off-state output current	V_{IN} = V_{OUT} = 0 V	0		50	µA
$I_{L(off2)}$	Off-state output current	V_{IN} = 0 V; V_{OUT} = 3.5 V	-75		0	µA
$I_{L(off3)}$	Off-state output current	V_{IN} = V_{OUT} = 0 V; V_{CC} = 13 V; T_j = 125 °C			5	µA
$I_{L(off4)}$	Off-state output current	V_{IN} = V_{OUT} = 0 V; V_{CC} = 13 V; T_j = 25 °C			3	µA

1. V_{CLAMP} and V_{OV} are correlated. Typical difference is 5 V.

Table 6. Switching (V_{CC} = 13 V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	R_L = 1.3 Ω (see *Figure 4*)		50		µs
$t_{d(off)}$	Turn-off delay time	R_L = 1.3 Ω (see *Figure 4*)		50		µs
$dV_{OUT}/dt_{(on)}$	Turn-on voltage slope	R_L = 1.3 Ω (see *Figure 4*)	See *Figure 15*			V/µs
$dV_{OUT}/dt_{(off)}$	Turn-off voltage slope	R_L = 1.3 Ω (see *Figure 4*)	See *Figure 16*			V/µs

Table 7. Logic inputs

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input low level voltage				1.25	V
I_{IL}	Low level input current	V_{IN} = 1.25 V	1			µA
V_{IH}	Input high level voltage		3.25			V
I_{IH}	High level input current	V_{IN} = 3.25 V			10	µA
$V_{I(hyst)}$	Input hysteresis voltage		0.5			V
V_{ICL}	Input clamp voltage	I_{IN} = 1 mA I_{IN} = - 1 mA	6	6.8 -0.7	8	V V

Table 8. V_{CC} output diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_F	Forward on voltage	- I_{OUT} = 5.3 A; T_j = 150 °C	-	-	0.6	V

Table 9. Protections(1)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
T_{TSD}	Shutdown temperature		150	175	200	°C
T_R	Reset temperature		135			°C
T_{hyst}	Thermal hysteresis		7	15		°C
I_{lim}	DC short circuit current	V_{CC} = 13 V 5 V < V_{CC} < 36 V	30	45	75 75	A A
V_{demag}	Turn-off output clamp voltage	I_{OUT} = 2 A; V_{IN} = 0 V; L = 6 mH	V_{CC} - 41	V_{CC} - 48	V_{CC} - 55	V
V_{ON}	Output voltage drop limitation	I_{OUT} = 1 A; T_j = -40 °C...150 °C		50		mV

1. To ensure long term reliability under heavy over-load or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device operates under abnormal conditions this software must limit the duration and number of activation cycles.

Table 10. Current sense[1]

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
K_1	I_{OUT}/I_{SENSE}	I_{OUT} = 1 A; V_{SENSE} = 0.5 V; T_j = -40 °C...150 °C	3300	4400	6000	
dK_1/K_1	Current sense ratio drift	I_{OUT} = 1 A; V_{SENSE} = 0.5 V; T_j = - 40 °C...150 °C	-10		+10	%
K_2	I_{OUT}/I_{SENSE}	I_{OUT} = 10 A; V_{SENSE} = 4 V; T_j = - 40 °C T_j = 25 °C...150 °C	4200 4400	4900 4900	6000 5750	
dK_2/K_2	Current sense ratio drift	I_{OUT} = 10 A; V_{SENSE} = 4 V; T_j = -40 °C...150 °C	-8		+8	%
K_3	I_{OUT}/I_{SENSE}	I_{OUT} = 30 A; V_{SENSE} = 4 V; T_j = -40 °C T_j = 25 °C...150 °C	4200 4400	4900 4900	5500 5250	
dK_3/K_3	Current sense ratio drift	I_{OUT} = 30 A; V_{SENSE} = 4 V; T_j = -40 °C...150 °C	-6		+6	%
I_{SENSE0}	Analog sense leakage current	V_{CC} = 6...16 V; I_{OUT} = 0 A; V_{SENSE} = 0 V; T_j = -40 °C...150 °C	0		10	µA
V_{SENSE}	Max analog sense output voltage	V_{CC} = 5.5 V; I_{OUT} = 5 A; R_{SENSE} = 10 kΩ V_{CC} > 8 V, I_{OUT} = 10 A; R_{SENSE} = 10 kΩ	2 4			V V
V_{SENSEH}	Sense voltage in overtemperature condition	V_{CC} = 13 V; R_{SENSE} = 3.9 kΩ		5.5		V
$R_{VSENSEH}$	Analog sense output impedance in overtemperature condition	V_{CC} = 13 V; T_j > T_{TSD}; output open		400		Ω
t_{DSENSE}	Current sense delay response	To 90 % I_{SENSE}[2]			500	µs

1. 9 V ≤ V_{CC} ≤ 16 V.
2. Current sense signal delay after positive input slope.

Table 11. Truth table

Conditions	Input	Output	Sense
Normal operation	L H	L H	0 Nominal
Overtemperature	L H	L L	0 V_{SENSEH}
Undervoltage	L H	L L	0 0
Overvoltage	L H	L L	0 0
Short circuit to GND	L H H	L L L	0 (T_j<T_{TSD}) 0 (T_j>T_{TSD}) V_{SENSEH}
Short circuit to V_{CC}	L H	H H	0 < Nominal
Negative output voltage clamp	L	L	0

Table 12. Electrical transient requirements on V_{CC} pin (part 1)

ISO T/R 7637/1 test pulse	Test levels				
	I	II	III	IV	Delays and impedance
1	- 25V	- 50 V	- 75 V	- 100 V	2 ms, 10 Ω
2	+ 25 V	+ 50 V	+ 75V	+ 100V	0.2 ms, 10 Ω
3a	- 25 V	- 50 V	- 100 V	- 150 V	0.1 µs, 50 Ω
3b	+ 25 V	+ 50 V	+ 75 V	+ 100 V	0.1 µs, 50 Ω
4	- 4 V	- 5 V	- 6 V	- 7 V	100 ms, 0.01 Ω
5	+ 26.5 V	+ 46.5 V	+ 66.5 V	+ 86.5 V	400 ms, 2 Ω

Table 13. Electrical transient requirements on V_{CC} pin (part 2)

ISO T/R 7637/1 test pulse	Test levels results			
	I	II	III	IV
1	C	C	C	C
2	C	C	C	C
3a	C	C	C	C
3b	C	C	C	C
4	C	C	C	C
5	C	E	E	E

Table 14. Electrical transient requirements on V_{CC} pin (part 3)

Class	Contents
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device is not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

Figure 4. Switching characteristics (resistive load R_L= 1.3 Ω)

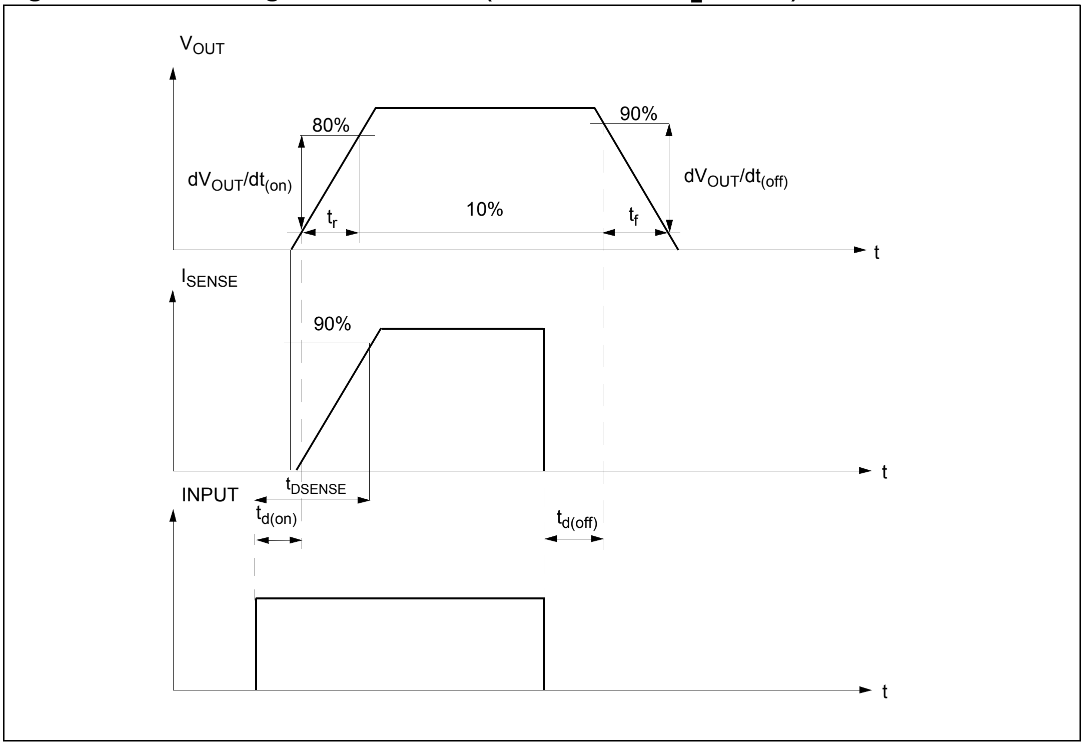


Figure 5. I_{OUT}/I_{SENSE} versus I_{OUT}

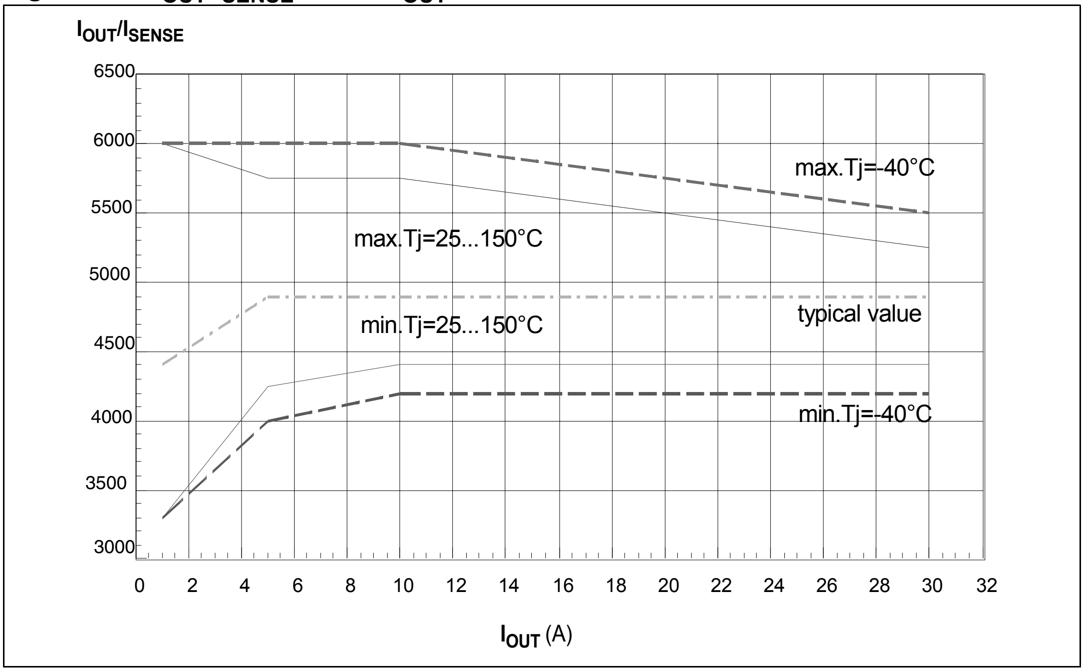
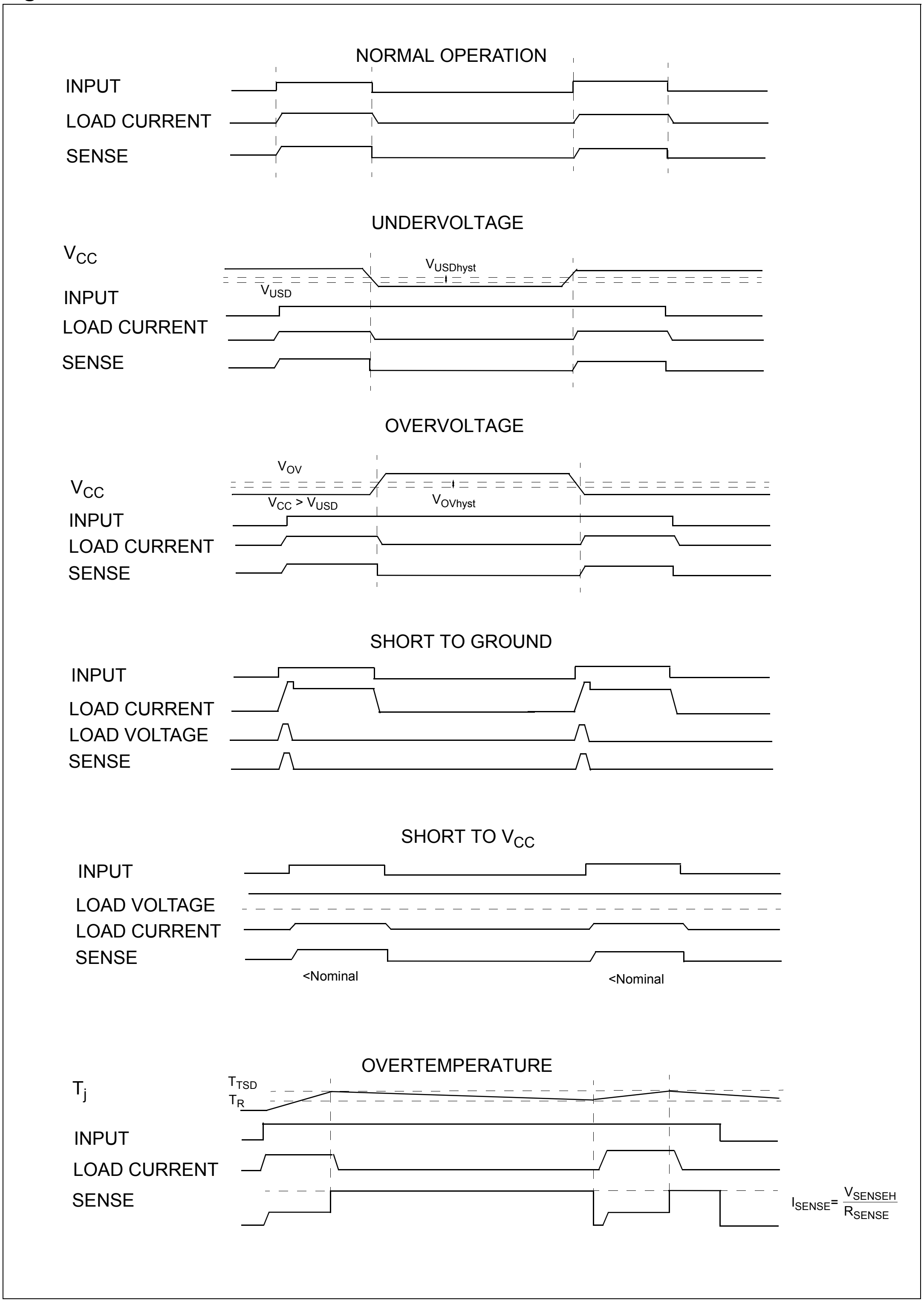


Figure 6. Waveforms



2.4 Electrical characteristics curves

Figure 7. Off-state output current

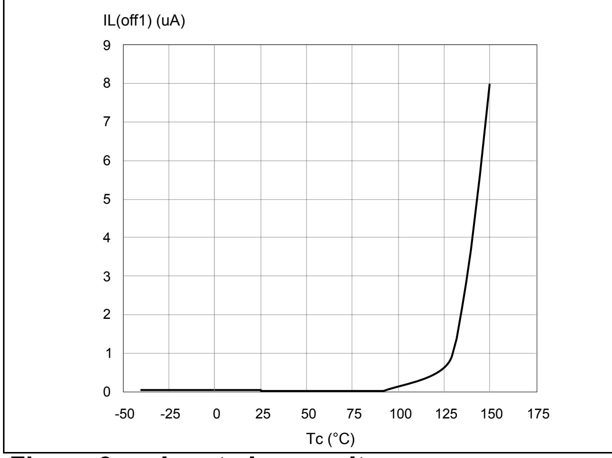


Figure 8. High level input current

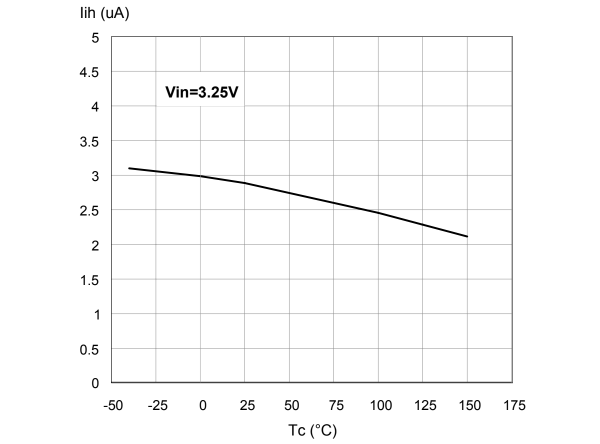


Figure 9. Input clamp voltage

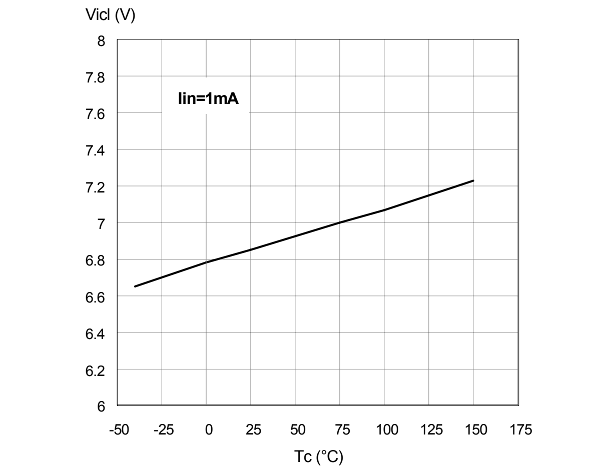


Figure 10. On-state resistance vs V_{CC}

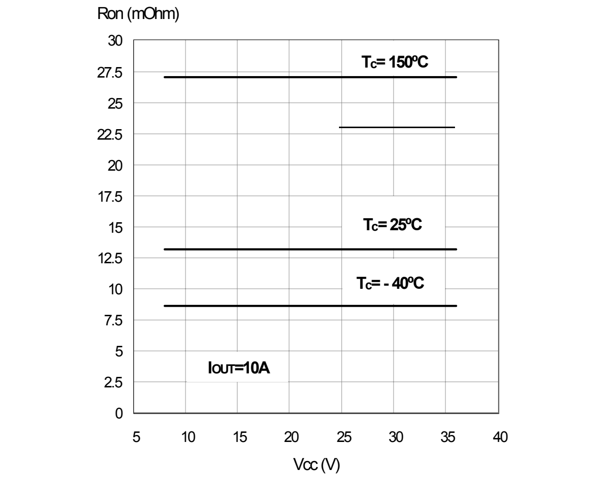


Figure 11. On-state resistance vs T_{case}

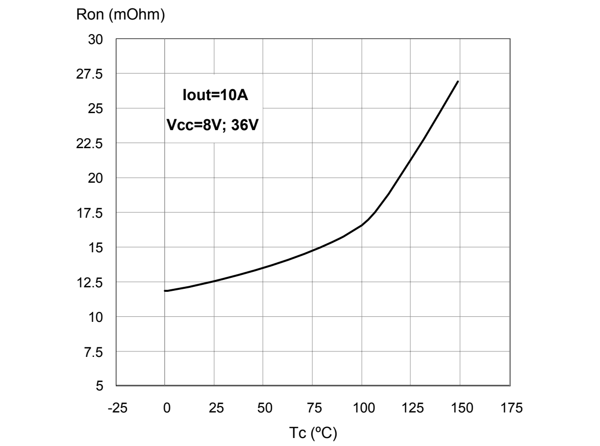


Figure 12. Input high level

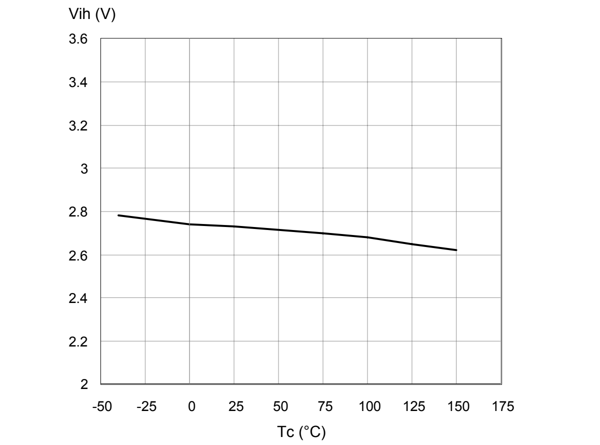


Figure 13. Input low level

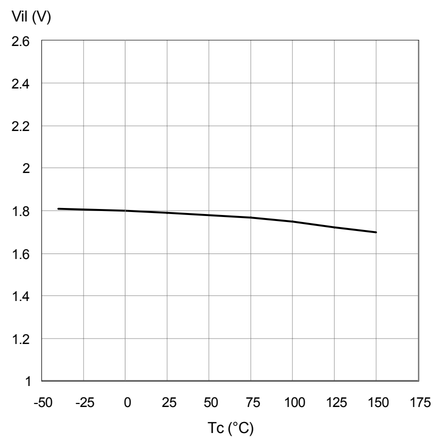


Figure 14. Input hysteresis voltage

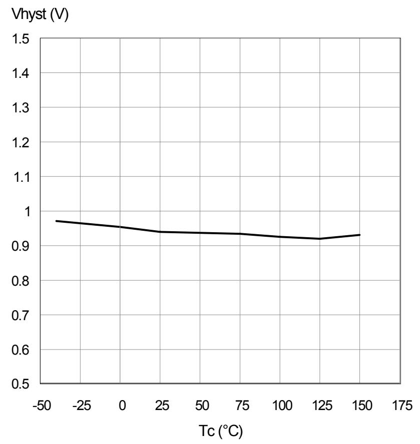


Figure 15. Turn-on voltage slope

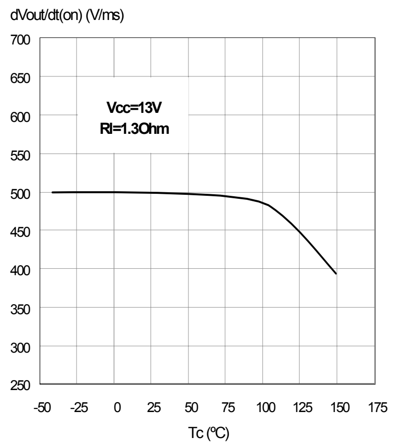


Figure 16. Turn-off voltage slope

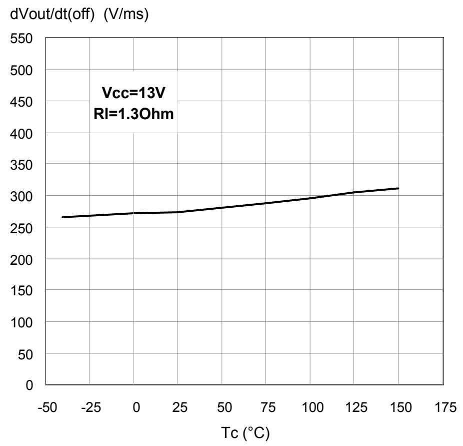


Figure 17. Overvoltage shutdown

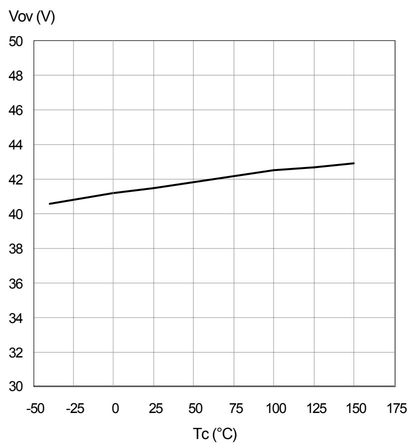
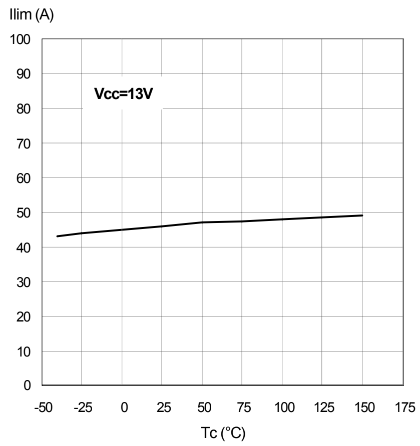
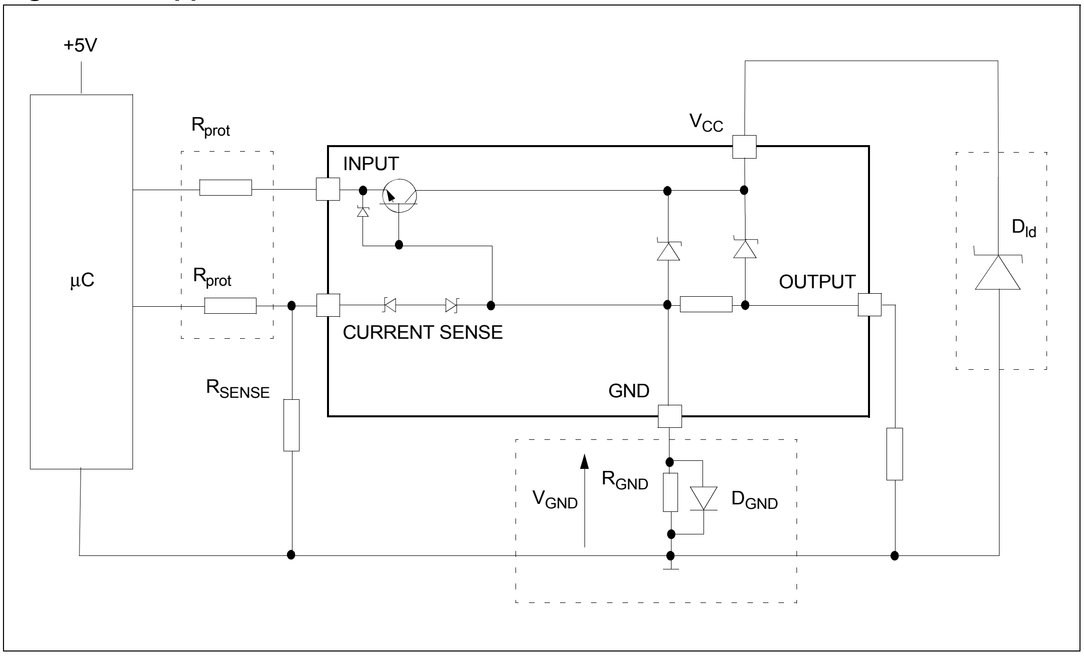


Figure 18. I_{LIM} vs T_{case}



3 Application information

Figure 19. Application schematic



3.1 GND protection network against reverse battery

3.1.1 Solution 1: resistor in the ground line (R_{GND} only)

This can be used with any type of load.

The following is an indication on how to dimension the R_{GND} resistor.

1. $R_{GND} \leq 600\ mV / (I_{S(on)max})$
2. $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where - I_{GND} is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device's datasheet.

Power dissipation in R_{GND} (when $V_{CC} < 0$: during reverse battery situations) is:

$P_D= (-V_{CC})^2/ R_{GND}$

This resistor can be shared amongst several different HSDs. Please note that the value of this resistor should be calculated with formula (1) where $I_{S(on)max}$ becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not shared by the device ground then the R_{GND} produces a shift ($I_{S(on)max}$ * R_{GND}) in the input thresholds and the status output values. This shift varies depending on how many devices are ON in the case of several high-side drivers sharing the same R_{GND}.

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then ST suggests to utilize solution 2 (see *Section 3.1.2*).

3.1.2 Solution 2: diode (D_{GND}) in the ground line

A resistor (R_{GND} = 1 kΩ) should be inserted in parallel to D_{GND} if the device drives an inductive load.

This small signal diode can be safely shared amongst several different HSDs. Also in this case, the presence of the ground network produces a shift (~600mV) in the input threshold and in the status output values if the microprocessor ground is not common to the device ground. This shift does not vary if more than one HSD shares the same diode/resistor network.

Series resistor in INPUT and STATUS lines are also required to prevent that, during battery voltage transient, the current exceeds the absolute maximum rating.

Safest configuration for unused INPUT and STATUS pin is to leave them unconnected, while unused SENSE pin has to be connected to ground pin.

3.2 Load dump protection

D_{ld} is necessary (Voltage Transient Suppressor) if the load dump peak voltage exceeds the V_{CC} max DC rating. The same applies if the device is subject to transients on the V_{CC} line that are greater than the ones shown in *Table 12*.

3.3 MCU I/Os protection

If a ground protection network is used and negative transient are present on the V_{CC} line, the control pins is pulled negative. ST suggests to insert a resistor (R_{prot}) in line to prevent the microcontroller I/Os pins to latch-up.

The value of these resistors is a compromise between the leakage current of microcontroller and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of microcontroller I/Os.

$-V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C}-V_{IH}-V_{GND}) / I_{IHmax}$

Calculation example:

For V_{CCpeak} = -100 V and $I_{latchup} \geq$ 20 mA; $V_{OH\mu C} \geq$ 4.5 V

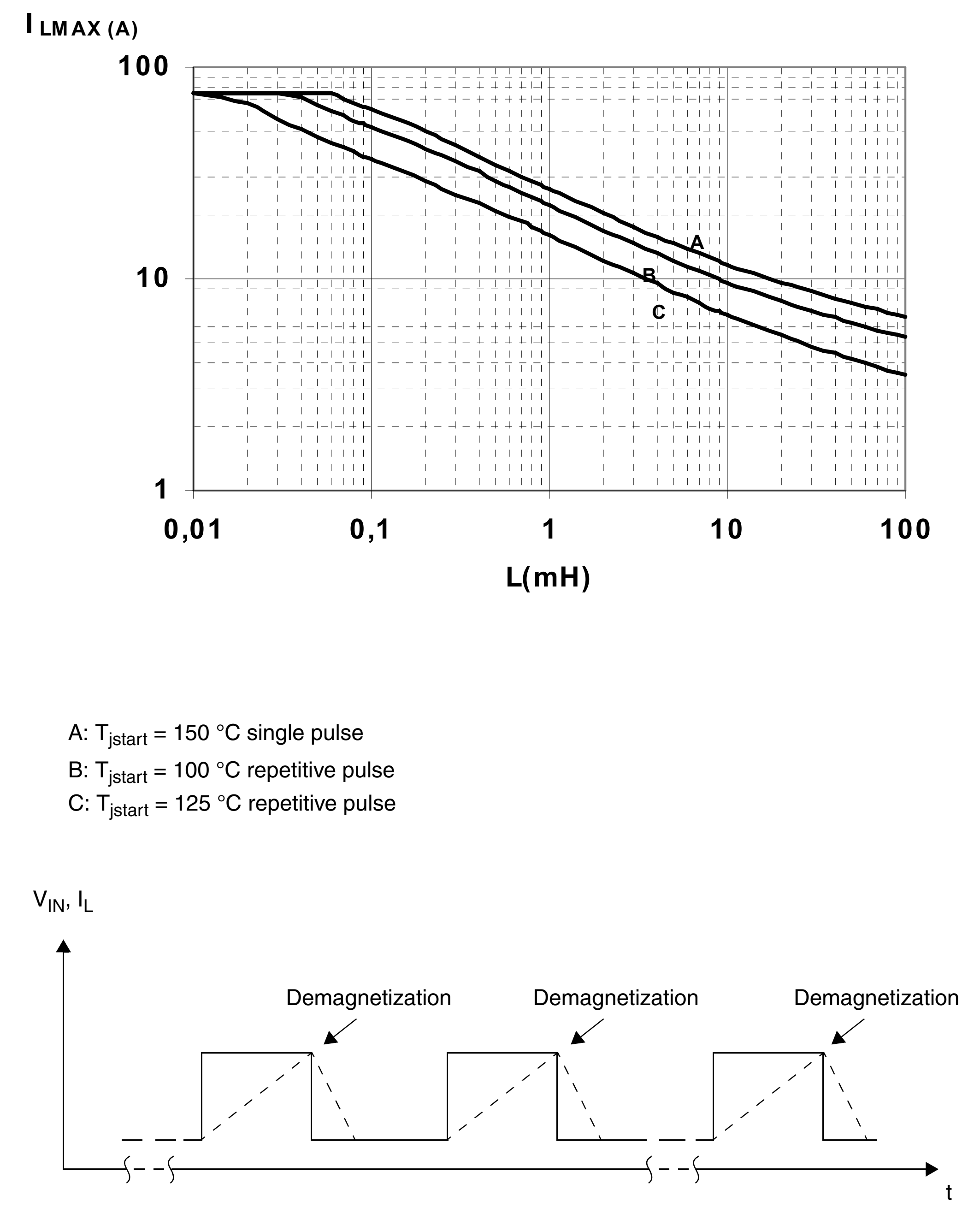
5 kΩ ≤ R_{prot} ≤ 65 kΩ.

Recommended values:

R_{prot} = 10 kΩ.

3.4 PowerSO-10 maximum demagnetization energy (V_{CC} = 13.5 V)

Figure 20. PowerSO-10 maximum turn-off current versus inductance

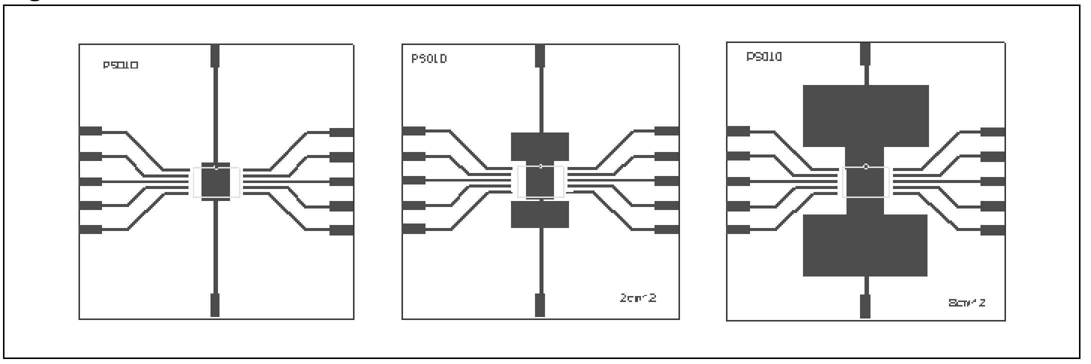


Note: Values are generated with R_L = 0 Ω. In case of repetitive pulses, T_{jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves B and C.

4 Package and PCB thermal data

4.1 PowerSO-10 thermal data

Figure 21. PowerSO-10 PC board



Note: Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area = 58 mm x 58 mm, PCB thickness = 2 mm, Cu thickness = 35 µm, Copper areas: from minimum pad layout to 8 cm^2).

Figure 22. $R_{thj-amb}$ vs PCB copper area in open box free air condition

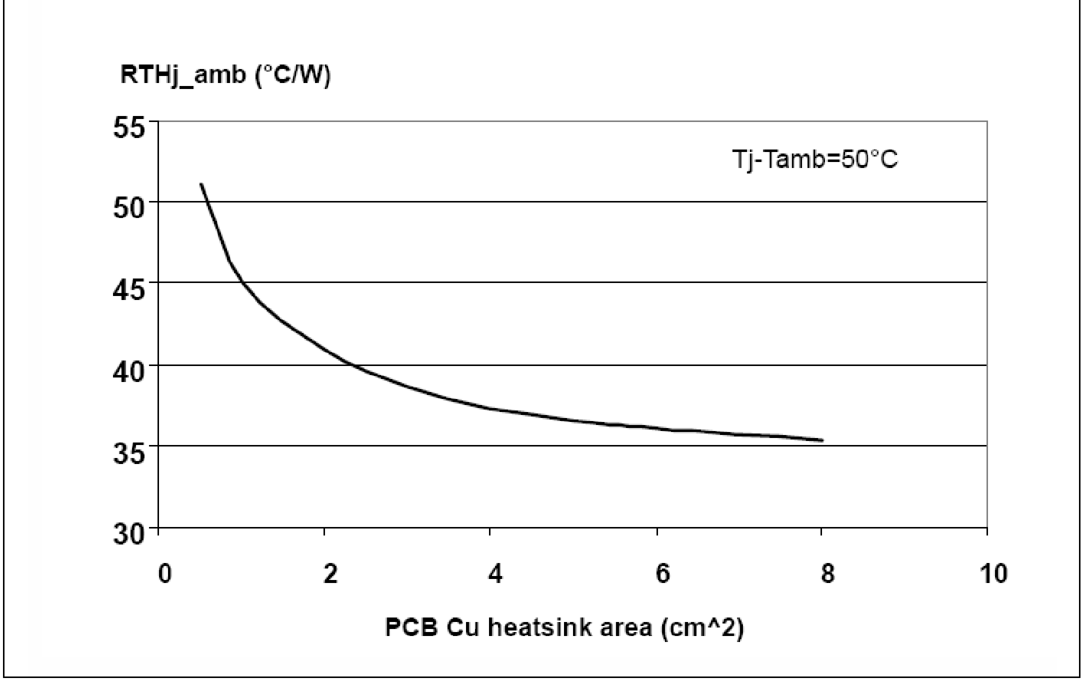
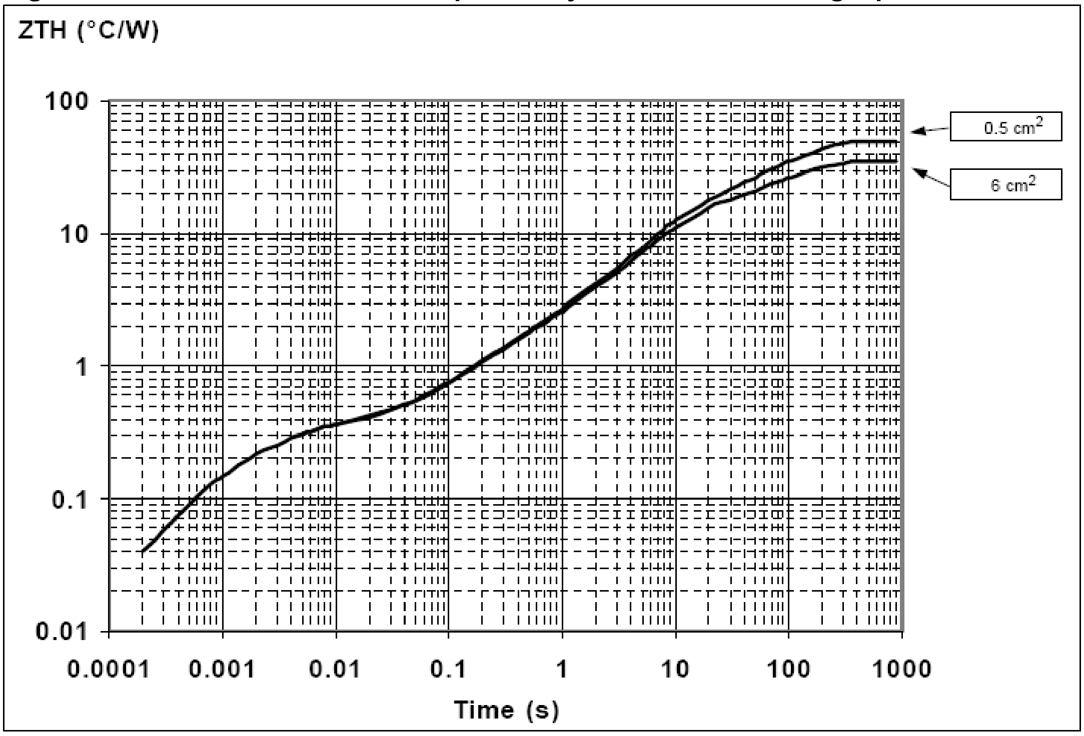


Figure 23. PowerSO-10 thermal impedance junction ambient single pulse



Equation 1: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p / T$

Figure 24. Thermal fitting model of a single channel HSD in PowerSO-10

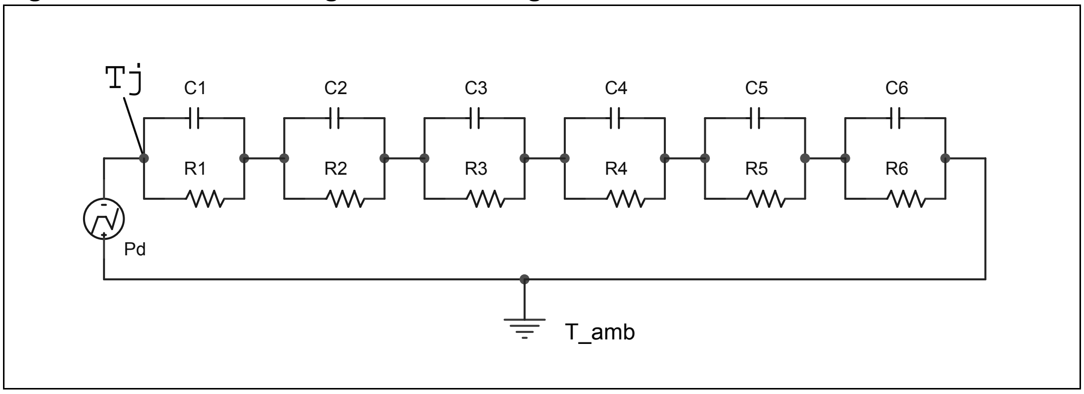


Table 15. Thermal parameters

Area / island (cm^2)	Footprint	6
R1 (°C/W)	0.02	
R2 (°C/W)	0.1	
R3 (°C/W)	0.2	
R4 (°C/W)	0.8	
R5 (°C/W)	12	
R6 (°C/W)	37	22
C1 (W.s/°C)	0.0015	
C2 (W.s/°C)	7.00E-03	
C3 (W.s/°C)	0.015	
C4 (W.s/°C)	0.3	
C5 (W.s/°C)	0.75	
C6 (W.s/°C)	3	5

5 Package and packing information

5.1 ECOPACK® packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

5.2 PowerSO-10 mechanical data

Figure 25. PowerSO-10 package dimensions

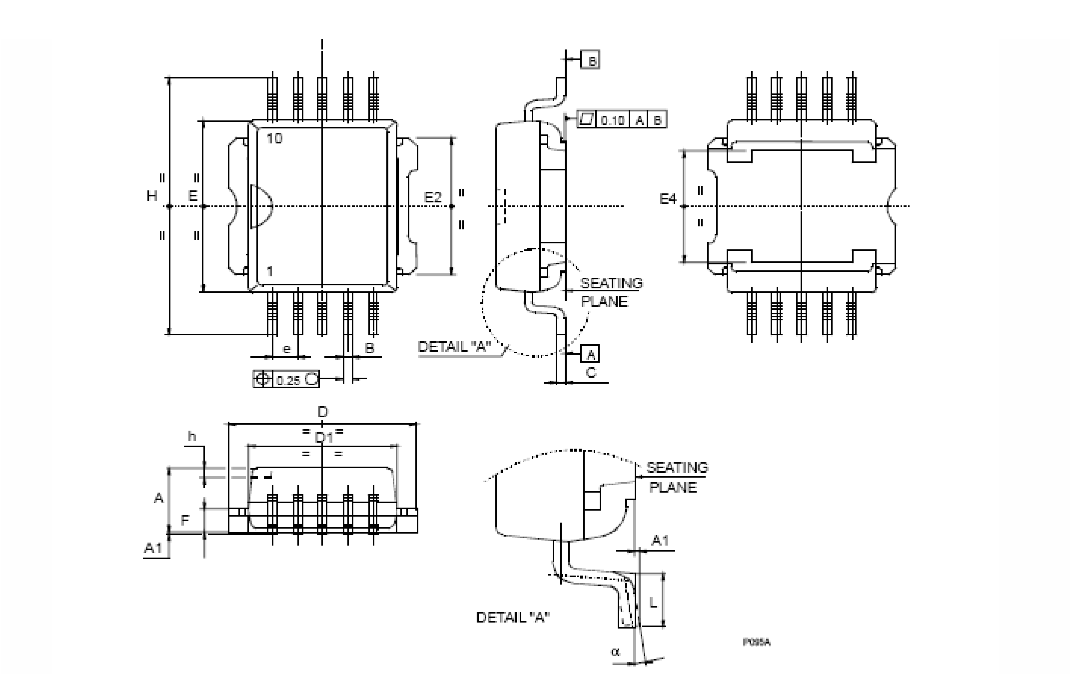


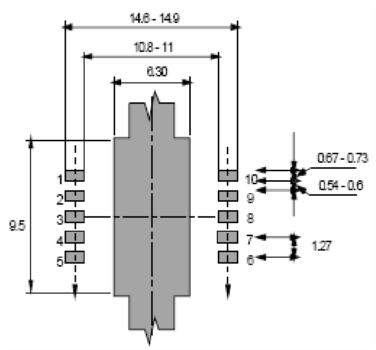
Table 16. PowerSO-10 mechanical data

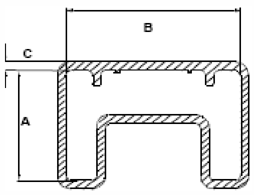
Dim.	Millimeters		
	Min.	Typ.	Max.
A	3.35		3.65
A[(1)]	3.4		3.6
A1	0.00		0.10
B	0.40		0.60
B[(1)]	0.37		0.53
C	0.35		0.55
C[(1)]	0.23		0.32
D	9.40		9.60
D1	7.40		7.60
E	9.30		9.50
E2	7.20		7.60
E2[(1)]	7.30		7.50
E4	5.90		6.10
E4[(1)]	5.90		6.30
e		1.27	
F	1.25		1.35
F[(1)]	1.20		1.40
H	13.80		14.40
H[(1)]	13.85		14.35
h		0.50	
L	1.20		1.80
L[(1)]	0.80		1.10
a	0°		8°
α[(1)]	2°		8°

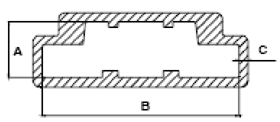
1. Muar only POA P013P.

5.3 PowerSO-10 packing information

Figure 26. PowerSO-10 suggested pad layout and tube shipment (no suffix)



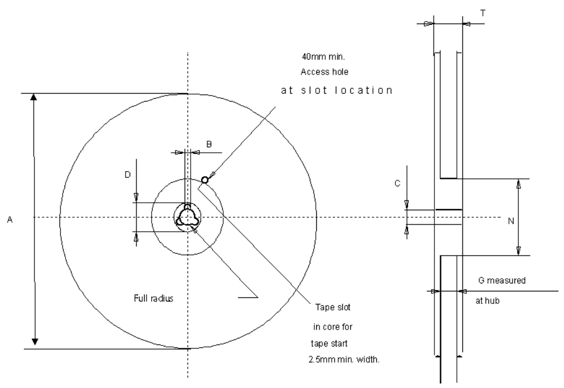




All dimensions are in mm.

	Base Q.ty	Bulk Q.ty	Tube length (± 0.5)	A	B	C (± 0.1)
Casablanca	50	1000	532	10.4	16.4	0.8
Muar	50	1000	532	4.9	17.2	0.8

Figure 27. PowerSO-10 tape and reel shipment (suffix “TR”)



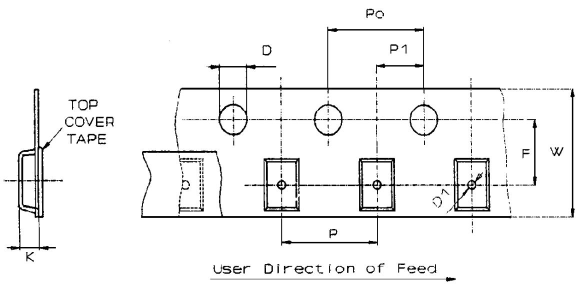
Reel dimensions

Base Q.ty	600
Bulk Q.ty	600
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	24.4
N (min)	60
T (max)	30.4

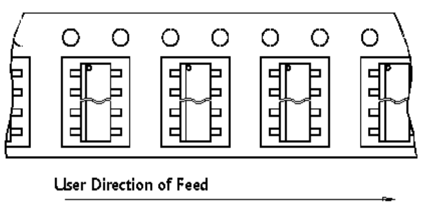
Tape dimensions

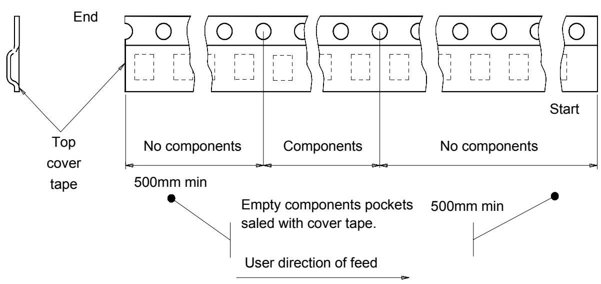
According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb. 1986

Tape width	**W**	24
Tape hole spacing	**P0 (± 0.1)**	4
Component spacing	**P**	24
Hole diameter	**D (± 0.1/-0)**	1.5
Hole diameter	**D1 (min)**	1.5
Hole position	**F (± 0.05)**	11.5
Compartment depth	**K (max)**	6.5
Hole spacing	**P1 (± 0.1)**	2



All dimensions are in mm.





6 Revision history

Table 17. Document revision history

Date	Revision	Changes
01-Oct-2004	1	Initial release.
17-May-2010	2	Updated *Features* list.
07-Feb-2011	3	Updated *Table 6: Switching (V_{CC} = 13 V)*